*Journal of Modern Science and Technology*
*Vol.2 No.1 March 2014. Pp.120-127*

# Power Aware Synthesis of Power Gated FSM

Priyanka Choudhury[1] and Sambhu Nath Pradhan[2]

*Power gating is often used to reduce power of a system which is in the form of a finite state machine (FSM). Power gating can be applied to turn OFF the inactive sub-machine which is obtained after partitioning the FSM by gating the supply voltage. Adjustment of supply voltage of one submachine for ON to OFF or OFF to ON state needs time, called wakeup time which affects the partitioning of FSMs for its power gated implementation as both the sub-machines are ON during this time. In this paper, we have calculated this wakeup time to find the number of clock cycles needed to activate the sub-machine. Power model based on state probability has been developed for the power-gated design of FSM. As effective partitioning and encoding of FSM decides the power consumption of final power gating implementation, in this paper Genetic Algorithm (GA) has been used to solve this integrated problem of both bi-partitioning and encoding. Experimental results obtained show the effectiveness of this approach. Affects of size of sleep transistor and sub-machine on the boundary depth have also been studied.*

**Field of Research**: Low Power VLSI Design.

## 1. Introduction

Nowadays device size is shrinking day by day and together with the larger number of devices on a die, results in an overall increase in power dissipation. So, there is a strong necessity for minimizing power consumption when designing complex microelectronic digital circuits and systems. In the absence of low-power design techniques then, current and future portable devices will suffer from either a very short battery life or a very heavy battery pack. There also exists a strong pressure for producers of high-end products to reduce their power consumption.

Most of the emerging computing devices and wireless communication systems require high speed computation and complex functionality with low power consumption and they are also control dominated. The controllers continue to run even when parts of data path are shut down. So, good amount of system power is consumed by the controller. Since most of the controllers are implemented as FSMs, power efficient synthesis of FSM has come up as a very important problem domain. An FSM can be partitioned into two or more coupled sub-machines such that most of the time only one of the sub-machines is active. The other sub-machine which is inactive does not consume any power. Logic minimization after suitable encoding can help to achieve a better realization in terms of area and power.

The power can further be reduced by applying power gating technique. Power gating is a technique for saving both leakage and switching power by shutting OFF the idle blocks of the circuit. Power efficiency of the power gated design depends on the

Priyanka Choudhury1, Department of ECE, NIT Agartala, Agartala, Tripura-799055, India.
Email: [1]priyanka.choudhury22@gmail.com
Sambhu Nath Pradhan, Department of ECE, NIT Agartala, Agartala, Tripura-799055, India.
Email: [2]sambhu.pradhan@gmail.com

wakeup time of the supply voltage. Again, this wakeup time depends on size of the sleep transistor and on size of sub-machine. In this paper, after suitably modifying the power metric of power gated FSM, we have considered partitioning and state encoding together for low power realization of FSM. The contributions of this paper are as follows:

(i) First time ever, boundary depth determination from wakeup time for different benchmark circuit has been presented.
(ii) The power model presented in (Pradhan, Tilak Kumar & Chattopadhyay 2011) has been modified to accommodate power consumption during cross transition.
(iii) GA based approach for simultaneous partitioning and state encoding of FSMs with power reduction as the objective using power gating.
(iv) Effectiveness of our encoding technique has been established by comparing the results with that of NOVA encoding (Villa & Vincentell 1990).
(v) Dynamic power consumed by the combinational part of the circuit, has been estimated by our power estimator at 45nm technology and compared with NOVA encoding (Villa & Vincentell 1990).
(vi) Power calculation is done considering the boundary depths which is 1 or 2 depending on the size of sleep transistor circuit, whereas, during power calculation in (Pradhan, Tilak Kumar & Chattopadhyay 2011), only boundary depth 2 was considered without any justification.
(vii) CPU computation time, which was not recorded in (Pradhan, Tilak Kumar & Chattopadhyay 2011) has been reported in this work.

The rest of the paper is organized as follows: the accumulative detail of the previous works is portrayed as literature review in section 2. Section 3 presents partitioning of FSM and architecture for power gating implementation. In section 4 the process of steady state probability calculation is explained. Proposed power model of power gated FSM is described in section 5. Section 6 describes the genetic algorithm for partitioning and state encoding. Experimental results are presented in Section 7. Finally, Section 8 concludes the whole work along with the future scope.

## 2. Literature Review

Power saving can be done by using clock gating or power gating considering together the problem of partitioning and encoding of FSM. The clock gating technique for low power FSM decomposition has been reported in (Chow et al. 1996) (Monteiro & Oliveira 1998). In (Chen et al. 2005) the experimental results show that, compared to no power gating, the total power can be reduced to 35.22% and 15.68% by using ideal clock gating and ideal power gating respectively. This clearly shows the effectiveness of power gating over clock gating. The works in (Leverich et al. 2009) (Pakbaznia & Pedram 2009) (Choudhury & Pradhan 2012) address the design of a power gating structure with high performance in the active mode, low leakage and short wakeup time during standby mode. The authors in (Liu et al. 2005) present a power-gating technique for FSM decomposition targeting low power. In (Venkataraman, Reddy & Pomeranz 2003) a GA based approach for simultaneous partitioning and state assignment of FSMs with power reduction as the objective was presented. The authors in (Pradhan, Tilak Kumar & Chattopadhyay 2011) considered the problems of FSM decomposition and state encoding together, targeting low power dissipation in power-gating technique. In (Pradhan, Tilak Kumar

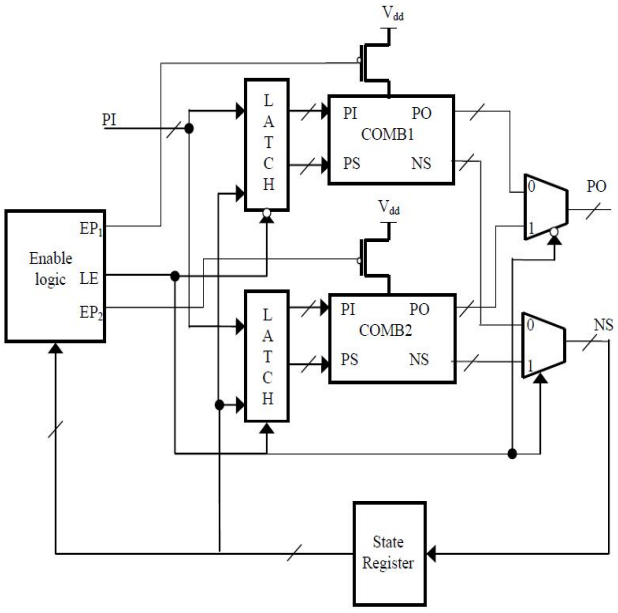
& Chattopadhyay 2011) during the cross transition power consumed by both the sub-machines was not considered. In this work we have modified the power model in (Pradhan, Tilak Kumar & Chattopadhyay 2011) to accommodate this power consumption. Here the power modeling is based on state probability, considering partitioning and state encoding together. Instead of taking boundary depth 2 (as in (Pradhan, Tilak Kumar & Chattopadhyay 2011)), if we take boundary depth 1, the boundary state probability may reduce as number of boundary states will reduce. However, there is no explanation why boundary depth 2 has been taken. In fact, for different circuit boundary depth will differs. So, we have determined boundary depth for each circuit first and then carried out experiments taking specific boundary depth of circuit.

## 3. Partitioning of FSM and Power Gating Implementation

Power gating technique was used in (Pradhan, Tilak Kumar & Chattopadhyay 2011) by adding a PMOS sleep transistor between $V_{dd}$ and the combinational circuit or by adding NMOS sleep transistor between combinational circuit and ground as shown in Fig.1 which is the proposed circuit architecture for power-gating in (Pradhan, Tilak Kumar & Chattopadhyay 2011). The same architecture is considered here. The description and partitioning strategy of the circuit was described in (Pradhan, Tilak Kumar & Chattopadhyay 2011).

Boundary depth (BD): It is defined as the number of clock cycles needed to turn ON the sub-machine to be activated.
Boundary states (BS): A boundary state between two sub-machines is a state in one sub-machine which is within the boundary depth of another machine. We use $D(F_1, F_2)$ to denote the set of boundary states in $F_1$ leading to $F_2$. The sum of the boundary state probability (BSP) of $D(F_1, F_2)$ is denoted as $P_D(F_1,F_2)$. Similarly, the sum of the boundary state probability of $D(F_2, F_1)$ is denoted as $P_D(F_2, F_1)$.

**Figure 1: Power-Gating Architecture**



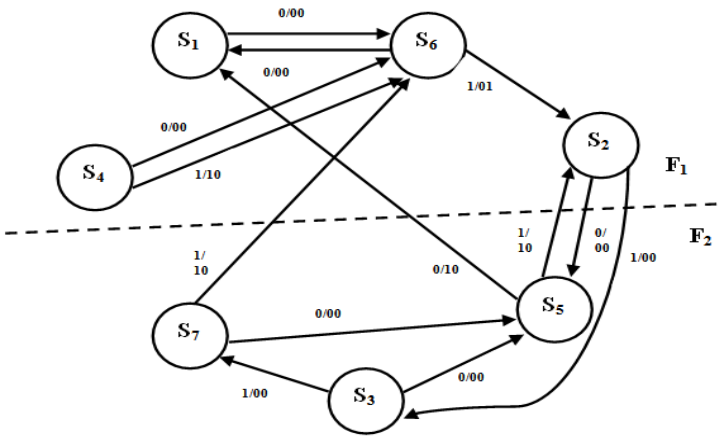
## 4. Power Modeling

Here we have used the same power model that has been used in (Choudhury & Pradhan 2012). We need this model only during the execution of the GA based partitioning and state assignment procedure that has been adopted in this paper.
Fig. 2 is an example of dk27 benchmark circuit showing the bipartitioning of a state transition graph (STG) into $F_1$ and $F_2$. For this example, the transitions between the states of $F_1 = \{S_1,S_2,S_4,S_6\}$ and the transitions between the states of the subFSM $F_2 = \{S_3, S_5, S_7\}$ are the inner transitions. The transitions from state $S_2$ to $S_3$, $S_2$ to $S_5$, $S_5$ to $S_2$, $S_5$ to $S_1$, $S_7$ to $S_6$ are the cross transitions. If the BD is taken as 2, then the set of BSs in the subFSM $F_1$ is $D_2(F_1, F_2) = \{S_2, S_6\}$ and for $F_2$, $D_2(F_2, F_1) = \{S_3, S_5, S_7\}$. BSP, $P_D(F_1, F_2) = P(S_2) + P(S_6) = 0.191+0.214 =0.405$ and $P_D(F_2, F_1) = P(S_3) + P(S_5) + P(S_7) = 0.095+0.167 + 0.047 = 0.309$ respectively. Calculation of $P(S_i)$ i.e Steady State Probability has been described in (Choudhury & Pradhan 2012). Developed power model contains four parts, each of which corresponds to a particular event based on the possible transitions. After combining the four parts we get,

$$Total\ power = P(F_1)Power(F_1) + P(F_2)Power(F_2) + P_D(F_1,F_2)\left[Power(F_1)+Power(F_2)\right] + P_D(F_2,F_1)\left[Power(F_1)+Power(F_2)\right] \quad (1)$$

where, the first term is due to power consumption of an inner transition which takes place in $F_1$, the second term is due to power consumption in of an inner transition which takes place in $F_2$, the third term is due to the cross transitions which takes place from $F_1$ to $F_2$ and the fourth term is due to cross transitions which takes place from $F_2$ to $F_1$.

**Figure 2: Bipartitioning of STG of dk27 Benchmark Circuit**




*Power estimation:* Power estimation is done by our power estimator (PE) after minimizing the PLA file by ESPRESSO (Brayton et al. 1985). For power estimation at 45nm technology we have used 1V supply. Node switching activity which is technology independent has been obtained after running *'print_power'* command of SIS (Sentovich et al. 1992). After simulation the original AND-OR PLA in Cadence Spectre, capacitance and delay have been noted as (Pradhan, kundu &

Chattopadhyay 2010) and accordingly dynamic power is estimated at 45nm technology by the following equation.

$$P = 0.5 x V_{dd} \text{^} 2 x sum( p x C ) / f \qquad (2)$$

where, $V_{dd}$ = 1V, $f$ = frequency of operation, $p$ = expected number of transitions of node $i$ in one clock cycle $i$, $C$ is the capacitive load of node $i$.

## 5. Genetic Algorithm for Partitioning and State Encoding

In this section, we present a solution strategy for the problem of simultaneous partitioning and encoding of FSM for the power gated design. GA (Goldberg & Hollend 1998) has the advantage of exploiting historical information to speculate on new search points with expected improved performance. It derives its behavior from a metaphor of natural selection and natural genetics by the creation of a population of individuals represented by artificial strings called chromosomes. The GA approach of partitioning and state encoding adopted here is same as (Pradhan, Tilak Kumar & Chattopadhyay 2011). But the fitness measure is done in the following way:

**Fitness Measure:**

The combinational logic parts corresponding to the two partitions are extracted, then minimized using ESPRESSO, and finally corresponding dynamic power values are computed. The values are then combined in Eq. (1) to compute the total power which is the fitness function of our GA based partitioning and state encoding.

## 6. Experimental Results

The proposed power-gating decomposition technique has been implemented in C language on a Pentium 4. We have estimated as explained in Section 5. For the set of benchmark circuits listed in Table 1, minimum operating frequency found to be 463 MHz.

Power consumption of sleep transistor of width 240nm is 0.18nw at 45nm technology. This power varies with different width of sleep transistor. Power of enable logic which is used to turn ON and OFF the sleep transistor is 2.2nw at 45nm technology. During power calculation these power values have been considered.
*Result after finding boundary depth (BD) of sub-machine:* In the experiment (Pradhan, Tilak Kumar & Chattopadhyay 2011), authors have considered that boundary depth is 2 but they did not fix the boundary depth for a particular sub-machine. In this section we set the boundary depth of a each sub-machine and apply the proposed power estimation technique explained in section 5. If a sub-machine is power-gated, the numbers of cycles which are needed to wake-up the sub-machine is the boundary depth for that sub-machine. The cost of the partitioned FSM is evaluated by the developed power model in the form of Eq.(1). In this power model boundary state probability is required to get the total power of the power gated FSM. This boundary state probability depends on the boundary depth of sub-machine. Different boundary depth of a same sub-machine gives different boundary state probability. So, first, we need to determine the boundary depth of a sub-machine and then partition the FSM using this power metric as cost. To find the boundary depth

before GA-based partitioning and encoding, we have taken GA encoded FSM. In a sub-machine maximum 80% states would be there as mentioned in Section 6. So, 80% encoded states of a FSM has been simulated in Cadence Spectre at 45nm technology to get the delay and wakeup time. The set of all the FSM after encoding has been simulated and delays and wakeup time are noted. Among all the delay, the maximum delay which is 2.16ns is taken to calculate the frequency of operation of all the sub-machine. So, the clock period is determined from the frequency of operation. For each circuit as we know the wakeup time and clock period, the boundary depth is determined after dividing wakeup time by clock period. Form Table 1 it is clear that for a particular size of sleep transistor wakeup time differs for different sub-machine and consequently boundary depth also varies for different sub-machine having different size. The size of the sleep transistor greatly affect the wakeup time for a particular sub-machine as shown in Table 1. We have shown the variation in boundary depth at 45nm technology for three different width ($w_1$ = 480nm, $w_2$ = 240nm and $w_3$ = 120nm) of sleep transistor keeping length fixed. The length and width are chosen such that boundary depth for the reported benchmark circuit is less than or equal to 2. Out of 18 circuits, the number of circuit having boundary depth 2 is 2, 5 and 8 at $w_1$, $w_2$ and at $w_3$ respectively. Average power saving of our power gated design over NOVA at $w_1$, $w_2$ and at $w_3$ is 49.52%, 48.55% and 46.17% respectively.

**Table 1: Wakeup Time, Boundary Depth and Power Saving for Different Size of Sleep Transistor**

| | wakeup time (ns) | | | boundary depth | | | % power saving over NOVA | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| circuits | $w_1$ | $w_2$ | $w_3$ | $w_1$ | $w_2$ | $w_3$ | $w_1$ | $w_2$ | $w_3$ | (Pradhan, Tilak Kumar & Chattopadhyay 2011) |
| bbara | 0.88 | 1.48 | 1.80 | 1 | 1 | 1 | 21.15 | 21.15 | 21.15 | 24.88 |
| cse | 1.48 | 2.38 | 2.89 | 1 | 2 | 2 | 62.45 | 49.39 | 49.39 | - |
| dk16 | 1.34 | 1.64 | 1.99 | 1 | 1 | 1 | 25.80 | 25.80 | 25.80 | 18.89 |
| dk512 | 0.7 | 1.02 | 1.24 | 1 | 1 | 1 | 49.53 | 49.53 | 49.53 | 52.51 |
| keyb | 1.46 | 1.788 | 2.17 | 1 | 1 | 2 | 80.63 | 80.63 | 72.18 | - |
| modulo12 | 0.41 | 0.702 | 0.85 | 1 | 1 | 1 | 48.55 | 48.55 | 48.55 | 19.23 |
| s1 | 1.72 | 1.902 | 2.31 | 1 | 1 | 2 | 43.19 | 43.19 | 16.17 | 29.4 |
| s208 | 1.22 | 1.44 | 1.75 | 1 | 1 | 1 | 57.89 | 57.89 | 57.89 | 37.37 |
| s386 | 1.1 | 1.32 | 1.61 | 1 | 1 | 1 | 71.61 | 71.61 | 71.61 | 51.13 |
| s510 | 2.18 | 2.208 | 2.68 | 2 | 2 | 2 | 64.91 | 64.91 | 64.91 | 61.57 |
| s820 | 2 | 2.162 | 2.63 | 1 | 2 | 2 | 79.68 | 78.70 | 78.70 | 78.34 |
| sand | 2.2 | 2.234 | 2.72 | 2 | 2 | 2 | 20.79 | 20.79 | 20.79 | 55.84 |
| bbtas | 0.382 | 0.66 | 0.80 | 1 | 1 | 1 | 37.43 | 37.43 | 37.43 | 17.31 |
| dk27 | 0.374 | 0.62 | 0.75 | 1 | 1 | 1 | 55.90 | 55.90 | 55.90 | 63.86 |
| planet | 1.82 | 2.14 | 2.60 | 1 | 1 | 2 | 57.26 | 57.26 | 49.90 | - |
| s832 | 2.08 | 2.18 | 2.65 | 1 | 2 | 2 | 78.83 | 75.44 | 75.44 | 77.32 |
| ex4 | 0.86 | 1.1 | 1.34 | 1 | 1 | 1 | 31.39 | 31.39 | 31.39 | 10.05 |
| donfile | 1.14 | 1.42 | 1.73 | 1 | 1 | 1 | 4.31 | 4.31 | 4.31 | 30.03 |
| AVERAGE | | | | | | | 49.52 | 48.55 | 46.17 | 41.85 |

*Result comparison with the literature:* Our power gated result is being compared with the result of (Pradhan, Tilak Kumar & Chattopadhyay 2011). It may be noted that power estimation in (Pradhan, Tilak Kumar & Chattopadhyay 2011) has been done by SIS (Sentovich et al. 1992) which is a quite old power estimator and technology is not mentioned. So, % saving of (Pradhan, Tilak Kumar & Chattopadhyay 2011) is being compared with this work. It may also be noted that in (Pradhan, Tilak Kumar & Chattopadhyay 2011) authors have developed the power model without considering power of both the sub-FSM when state is making transition from one sub-FSM to other and also they have considered boundary depth 2. In our work we have considered power of both the sub-FSM when there is a state transition from one to other sub-FSM. To account this effect, two extra terms $P_D(F_1,F_2)Power(F_1)$ and $P_D(F_2,F_1)Power(F_2)$ are considered in developing the power model (Eq. (1)), described in Section 5. Due to the presence of these additional terms in the power model (Eq. 1), the results are bit worse than the results in (Pradhan, Tilak Kumar & Chattopadhyay 2011) for the same boundary depth.

For boundary depth 2 our solution gives around 36% average saving, where as solution in (Pradhan, Tilak Kumar & Chattopadhyay 2011) shows around 42% saving with respect to NOVA. Average saving of our power gated design with boundary depth 1 is around 51% with respect to NOVA. This saving is more than the saving obtained using (Pradhan, Tilak Kumar & Chattopadhyay 2011) taking boundary depth 2. This is because for boundary depth 1, number of boundary state is less which results reduction in boundary state probability and the corresponding increase in saving. However, after fixing the boundary depth, the power result at $w_1$, $w_2$ and $w_3$, are better than the power result of (Pradhan, Tilak Kumar & Chattopadhyay 2011). This is because, not all the circuit at $w_1$, $w_2$ and $w_3$ has boundary depth 2, few have boundary depth 1. The comparison of power savings with respect to NOVA for techniques like (Pradhan, Tilak Kumar & Chattopadhyay 2011) and our approach considering boundary depth 1 are presented in the last column of Table 1.

## 7. Conclusions and Future Work

We have presented an efficient technique for synthesizing the FSMs using power-gating targeting dynamic power saving. The idea of combined partitioning and state encoding is introduced in the synthesis process in the genetic algorithm formulation. Existing power model has been modified to account the power consumption during cross transition. As boundary depth depends on wakeup time of sub-machine and this wakeup time differs for different size of the sleep transistor and sub-machines, for a particular size of sleep transistor, we have determined boundary depth. The technique worked well as verified by the experimentation with a number of benchmark circuits. Low power partitioning and encoding of FSM may increase the area of final circuit. Area result has not been reported in this work. Our future works include, doing experiments to find the impact of switching and leakage for this power gated design of a practical circuit. Clock gating may be applied to the proposed power gating architecture for further power reduction. The FSM partitioning can be extended to multipartitions. Effectiveness of this technique may be examined targeting multilevel circuit synthesis.

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