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Performance Evaluation of 8-Transistor and 9-Transistor, 32-Nm CNT-Opamps in Designing and Comparing Non-Inverting Amplifiers

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In this paper, we have presented the design and characteristic performance evaluation of two different Carbon Nanotube-based Operational Amplifiers (CNT-OPAMPs) using a benchmark eight-transistor and a nine-transistor OPAMP model with single-walled Carbon Nanotube Field-Effect Transistors (SW-CNTFETs) as primary building-blocks for 32nm technology. Our simulation-based assessment of a non-inverting amplifier has shown that for 8T configuration, excepting the CNT-FET with n=1, the devices with n=3 and n=5 showed considerable improved performance in all parameters except the input resistance. For a 9T configuration, all the CNT-FET based devices (n=1, n=3, and n=5) showed considerable improved performance than Si-based device in terms of Bandwidth, Output Resistance, Power Dissipation, and Gain-Bandwidth Product. The CNT-FET based device fell short just in terms of input resistance and phase margin. The DC Gain of both the Si-based as well as the CNT-FET based device was almost same. The results obtained suggest that the CNT-OPAMP has a promising potential for low-power, high-speed applications in both analog and mixed-signal nanoelectronic circuits.

Field of Research: Electrical and Electronic Engineering

1. Introduction

With the rapid advancement and growth of the semiconductor industry, our perception of the electronic world has now come to a new dimension with even smaller, faster and cheaper devices incorporating ground-breaking and novel technologies and it is still progressing. But this has certain limitations that must be addressed before further technological advancement. The foundation of the current technology is the Silicon-based Complementary Metal-Oxide Semiconductor (CMOS) devices that, following Moore's Law, has been scaled down to smaller dimensions for more than the past 30 years, and has showed better performances with even higher device density and lower power consumption. Addressing this continued down-scaling process, the International Technology Roadmap for Semiconductors (ITRS) report in 2009 states that further scaling down in current silicon-based VLSI technology has faced notable limitations in fabrication process and device performances along with approaching the fundamental limitations of Si-based material morphology as the critical device dimension is currently shrinking down to sub-22nm range, and thus ITRS makes a prediction that the progress of MOSFET scaling could meet an end sometime around 2018 with a sub-16nm node (International Technology Roadmap for Semiconductors 2009). Major drawbacks of such extensive scaling involve electron tunneling through short channels and thin insulator films

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resulting in high leakage currents and passive power dissipation, device structure mismatch, random doping fluctuations and mobility degradation (Avouris & Chen 2004). So it has been essential to introduce methods and innovative device structures to overcome these limitations and sustain the nanoelectronic VLSI manufacturing technology to advance with further possible device scaling down as well as to meet challenges like cost, consistency, speed, and performance.

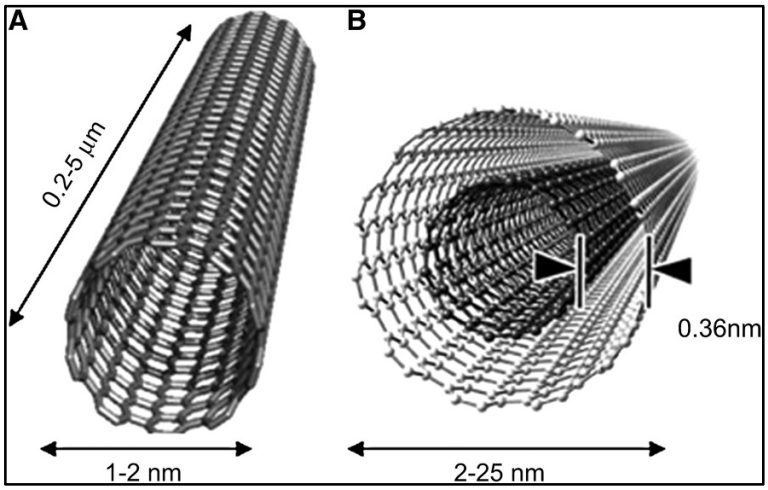
We have organized the rest of the paper as follows: a brief overview on the CNTFET models is given in section 2. Our study perspective, necessary circuits, and simulation configuration used for investigation purposes are described in section 3. The simulation results, obtained performance, and findings are presented in section 4. Finally our analysis is concluded in section 5 with the limitations and future prospects of our study.

2. Literature Review

One of the most promising alternative technology, to keep the future nanoelectronic VLSI manufacturing evolution in pace and make it even faster with better performance, is Carbon Nanotube (CNT) and CNT-based device technology. CNTs have emerged as the wonder materials of the era and are currently being considered for a wide range of applications, ranging from large scale automobile structures to even nano-scaled electronics (Bandaru 2007). Since the discovery of Multi-Walled Carbon Nanotubes (MWNTs) using a transmission electron microscope in 1991 (Ijima 1991) and the Single-Walled Carbon Nanotubes (SWNTs) two years later (Ijima & Ichihashi 1993); scientists have devoted themselves in growing, fabricating and characterizing different types of CNTs and CNT-based devices.

SWNTs can be considered equivalent to the wrapping of a one-atom-thick layer of graphite called ‘graphene’ into a seamless cylinder, with typical diameters on the order of single digit nanometers, and their lengths ranging from tens of nanometers to several centimeters as shown in Figure-1(A) in the next page. MWNTs consist of several such cylinders nested inside each other as shown in Figure-1(B) in the next page. Such large aspect ratio makes the nanotubes, especially SWNTs, nearly ideal one-dimensional (1-D) objects that practically result in 1-D ballistic transport, thus leading to potential benefit of much higher carrier mobility as compared to that of the bulk MOSFET. In addition, the detailed arrangement of the carbon atoms, or the chirality, makes a SWNT to be metallic or semiconducting, and thus enabling it to operate as necessary for designed nano-electronic devices and circuits (Sinha, Balijepalli & Cao 2008).

Figure 1: Carbon Nanotube Structures: (A) Single-Walled Nanotube, (B) Multi-Walled Nanotube



It is obvious that CNTs present a unique opportunity as one of the few systems where atomistic-based modeling may reach the experimental device size, thus in principle allowing the experimental validation of computational approaches and computational device design (O'Connell 2006). But the practical growth and fabrication of CNTs and CNT-based devices is quite complicated as obstacles remain in controlling proper chirality, specific and precise nanotube separation, and surface state control (Yeetsorn 2004). So we have focused on simulation for CNT devices, more specifically on CNTFETs and CNTFET-based analog filter circuits.

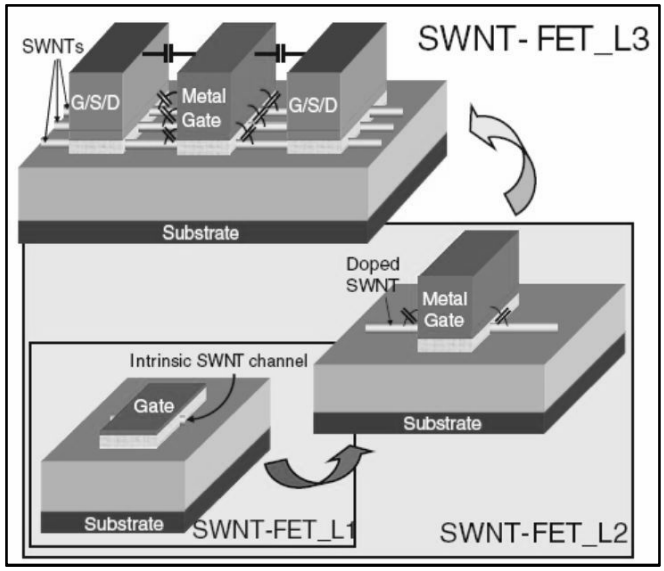
2.1 CNTFET Modeling Overview

Since the discovery of CNT, the major obstacles scientists have been facing are the complicated growth and fabrication mechanism of CNTs and CNT-devices, which in turn, made us look forward to make proper mathematical models which can represent their physical and electrical nature.

One of the major achievements was to design, fabricate and model CNTFETs. CNTFETs are field-effect transistors using properly designed CNTs in the intrinsic channel region under the metal Gate between the Drain and the Source of a conventional FET. Its equivalent circuit is quite similar to the common Si-based MOSFET, but the CNT channels result in higher speed and less power consumption compared to nanoscale conventional MOSFET**.** One of the earliest CNTFET models was One-dimensional ballistic model (Javey, Guo, Wang, Lundstrom & Dai 2003) which over-estimated the drain current. An improved version of the CNTFET model was proposed by researchers at the Stanford University in 2007 and has currently become popular for CAD based modelling (Deng & Wong 2007). As shown in Figure-2, it segments the CNTFET into three different levels with more non-ideality factors than the former level. Here SWNT-FET_L1 is the core of the model and describes the intrinsic SWNT channel region of the SWNT-FET. SWNT-FET_L2 models the source or drain extension regions and contacts. SWNT-FET_L3 shows the full SWNT-FET model allowing multiple nanotubes per device.

Many other studies have used this compact model as a benchmark and with minor alterations, if necessary (Usmani & Hasan 2009). In our study, we have also taken this model as the building-block for the characteristic analysis and performance evaluation for CNTFET based analog circuits (non-inverting amplifier).

Figure 2: The 3-Level Hierarchy of the Circuit-Compatible Compact SWNT-FET Device Model



3. Data and Methodology

In this paper, we have first studied and analyzed the characteristic performances of two different OPAMP models with different number of FETs. We simulated these to compare the performance between them for making a better selection in practical circuits. To do this, we first designed the OPAMPs using Si-FETs. Then we designed the analog circuit using the same Si-based OPAMPs. Then we evaluated the performance of the designed circuit by repeating the process using CNTFETs instead of Si-FETs and then compared the results of both type of devices. We further compared between the designed CNTFET-based devices by changing the number of CNTs in the intrinsic channel region of the CNTFETs.

3.1 CNTFET

In our study, we have used the Stanford circuit-compatible compact model for the intrinsic channel region of the MOSFET-like SWNT-CNTFET, for designing the CNT-OPAMP. The Stanford model is valid for a wide range of chiralities and diameters, and it also allows creating metallic or semiconducting channel. This model also includes a complete trans-capacitance network to deliver the real-time dynamic response for both large and small signal operations.

We have implemented all our required models in HSPICE. Necessary simulation parameters used for the CNTFETs are summarized in Table-1.

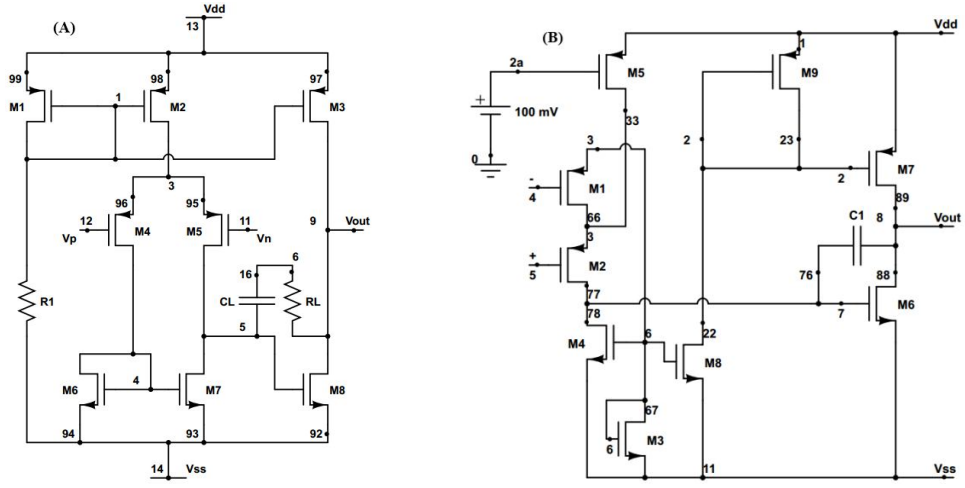
Table 1: CNTFET Parameters for Simulations

CNTFET Parameter	Type/Value
Chirality Type	Zigzag
Channel Length	32 nm
Diameter	1.5 nm
Pitch	20 nm
Sub-Pitch	6.4nm
Oxide Thickness (HfO_2)	4 nm
K (Dielectric Constant)	16

3.2 Eight-Transistor (8T) and Nine-Transistor (9T) CNT-OPAMP

We have used an eight-transistor benchmark model (OPAMP1) and a nine-transistor benchmark model (OPAMP2) for the design of the OPAMP as shown in Figure-3 in the following page (Kaminska, Arabi, Bell, Goteti, Huertas, Kim, Rueda & Soma 1997).

Figure 3: (A) Eight-Transistor OPAMP (OPAMP1) and (B) Nine-Transistor OPAMP (OPAMP2)



First, we have designed the OPAMPs with the mentioned circuit configurations by using Si-FETs. Then we replaced the Si-OPAMPs with CNT-OPAMPs. These CNT-OPAMPS have been designed using CNTFETs with three SWNTs (n=3) in the intrinsic channel region. We have compared both the results for better understanding of their performance. Then we further evaluated the circuit by changing the number of SWNTs in the intrinsic channel region (n=1, n=5).

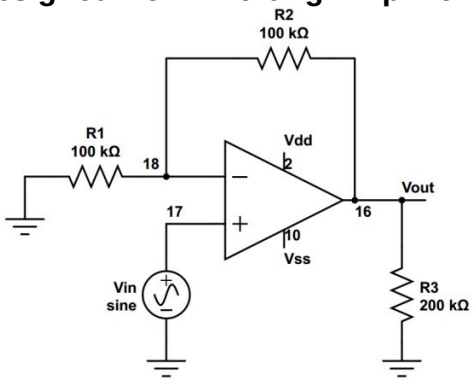
3.3 Circuit for Simulation

For the comparison analysis of CNT-OPAMPs with OPAMP1 and OPAMP2 configurations, we concentrated on the calculations of some characteristic parameters of the OPAMP such as Gain, Bandwidth, Phase Margin, Input and Output resistances, Gain-Bandwidth Product, and Power Consumption. We have obtained these results from a well-designed Non-inverting Amplifier configuration with a DC gain of two as shown in Figure-4 in the next page.

The non-inverting amplifier is called this because the input signal is connected to the non-inverting terminal. Also the output is in phase with the input.

A special case of the non-inverting amplifier is that of the Voltage Follower. The voltage follower has the output signal connected to the inverting input terminal of the OPAMP. The analysis of this device shows that $V_{out} = V_{in}$. The common use for a voltage follower is to create a buffer in a digital circuit. The follower isolates the output signal from the signal source with the very large input impedance. This is where the term 'buffer' came from. Its gain configuration is one of the most useful of all OPAMP stages, for several reasons. Because the V_{in} sees the OPAMP's high impedance (+) input, it provides an ideal interface to the driving source. Gain can easily be adjusted over a wide range via R1 and R2, with virtually no source interaction

Figure 4: The Designed Non-Inverting Amplifier for Evaluations



3.4 Observed Parameters

3.4.1 DC Gain

Gain is a measure of the ability of a circuit to increase the power or amplitude of a signal from the input to output. It is usually defined as the mean ratio of the signal output of a system to the signal input of the same system. When gain is greater than one, it is known as amplification.

Amplification is usually the property of active circuits, while passive circuits usually have a gain of less than one. Voltage gain is simply: Gain = V_{out} / V_{in}

3.4.2 Bandwidth

Bandwidth is the difference between the upper and lower frequencies in a continuous set of frequencies. It is usually measured in hertz (Hz). Depending on context, bandwidth sometime refers to pass-band and base-band. Pass-band is the difference between the upper and lower cut-off frequencies and base-band always refers to the upper cut-off frequency, regardless of the filter being band-pass or low-pass.

3.4.3 Gain-Bandwidth Product (GBP)

Gain-Bandwidth Product is the product of an amplifier's bandwidth and the gain at which the bandwidth is measured. From the gain and phase margin curves, GBP is the frequency at which the phase voltage is zero.

3.4.4 Phase Margin

Phase margin is the difference between the phase of an amplifier's output signal and 180°, as a function of frequency which is measured in degrees. Generally, phase margin is measured at the frequency where the open loop voltage gain of the amplifier equals the desired closed loop DC voltage gain.

3.4.5 Input Resistance

Input resistance is defined as the DC resistance between the input terminals with either input grounded.

3.4.6 Output Resistance

Output resistance is defined as the dc resistance that is placed in series with an ideal amplifier and the output terminal.

3.4.7 Total Power Dissipation

Total power dissipation is defined as the total dc power supplied to the device less any power delivered from the device to a load.

4. Findings and Discussion

In this section, we have provided the overall tabulated results and associated graphs of each of the circuits that we chose for our research purposes.

Table 2: Comparison between Conventional Si-MOSFET Based OPAMP1 and OPAMP2

Parameter	Unit	8-Transistor Si-MOSFET	9-Transistor Si-MOSFET
DC Gain		1.9977	1.8917
Input Resistance	Ω	1E20	1E20
Output Resistance	Ω	51.8938	4.1496K
Bandwidth	Hz	2.13M	10.5K
Phase Margin	Degrees	-54	-48.7
Power Dissipation	μW for 200 KΩ Load	57.8757	1.2144
Gain-Bandwidth Product (GBP)	Hz	4.255M	19.863K

From Table-2 in the previous page, we can see that OPAMP1 model based non-inverting amplifier is better than the OPAMP2 model based non-inverting amplifier in all aspects, excepting the phase margin.

Figure 5: Gain v/s. Frequency Curve of OPAMP1 Si-MOSFET and CNT-FET with n=3

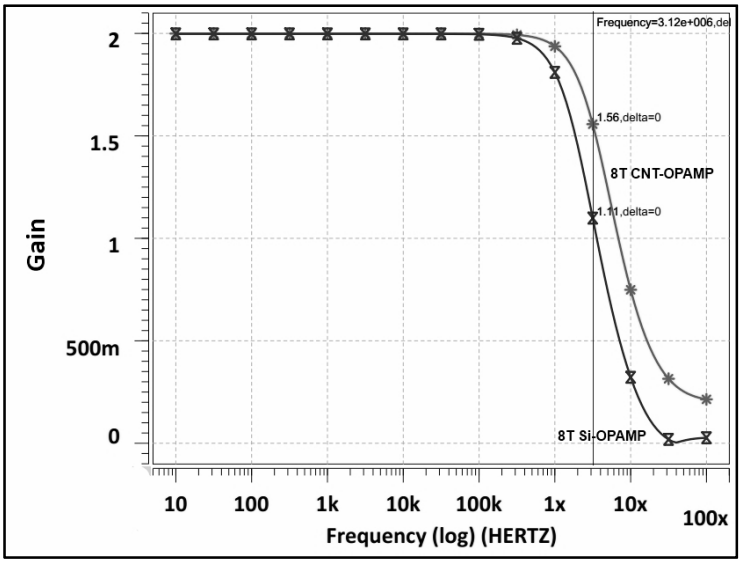


Table 3: OPAMP1: Comparison between Si-MOSFET based and CNTFET based Non-Inverting Amplifier

Parameter	Unit	8-Transistor Si-MOSFET	8-Transistor CNT-FET (3 Tubes)
DC Gain		1.9977	1.999
Input Resistance	Ω	1E20	1E12
Output Resistance	Ω	51.8938	11.64
Bandwidth	MHz	2.13	3.97
Phase Margin	Degrees	-54	-52.5
Power Dissipation	μW	57.8757 for 200 kΩ load	64.85 for 100 MΩ load
Gain-Bandwidth Product (GBP)	MHz	4.255	7.936

From Table-3 in the previous page, we can see that for OPAMP1, CNT-FET based non-inverting amplifier is better than the conventional Si-MOSFET based non-inverting amplifier in all aspects, excepting the input resistance.

Figure 6: Phase v/s. Frequency Curve of OPAMP1 Si-MOSFET and CNT-FET with n=3

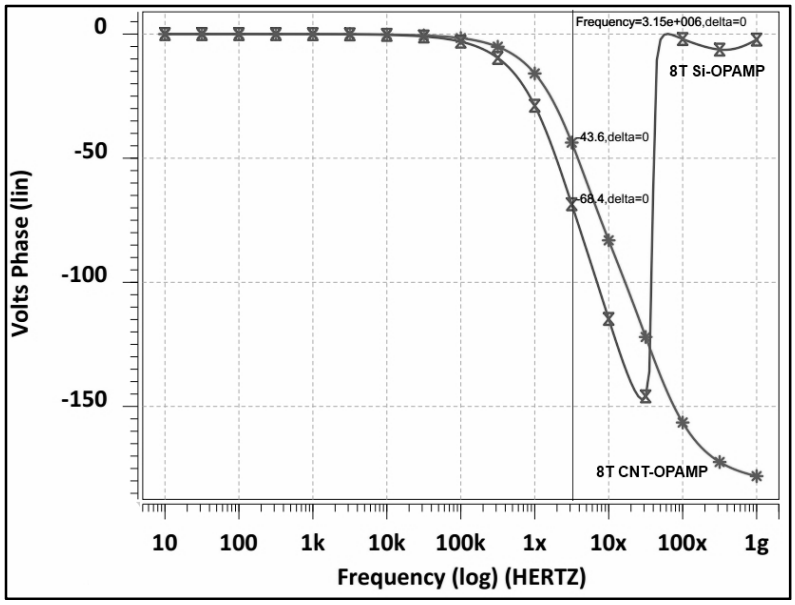


Table 4: Comparison between Si-MOSFET based and CNT-FET based Non-Inverting Amplifier

Parameter	Unit	9-Transistor Si-MOSFET	9-Transistor CNT-FET (3 Tubes)
DC Gain		1.8917	1.999
Input Resistance	Ω	1E20	1E12
Output Resistance	Ω	4.1496K	5.041
Bandwidth	Hz	10.5K	3.00M
Phase Margin	Degrees	-48.7	-104
Power Dissipation	μW	1.2144 for 200 kΩ load	204.4 for 100 MΩ load
Gain-Bandwidth Product (GBP)	Hz	19.863K	5.997M

From Table-4 in the previous page, we can see that for OPAMP2, CNTFET based non-inverting amplifier is better than the conventional Si-MOSFET based non-inverting amplifier in all aspects, excepting the phase margin and the input resistance.

Figure 7: Gain v/s. Frequency Curve of OPAMP2 Si-MOSFET and CNT-FET with n=3

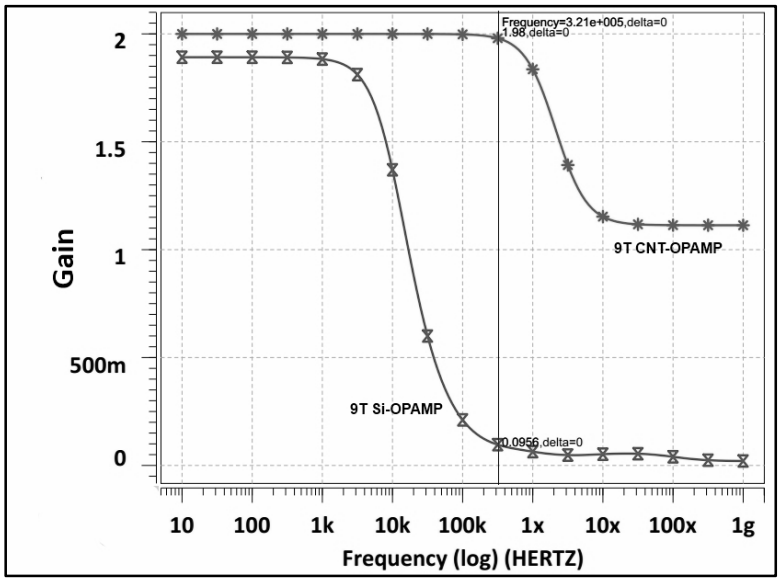


Table 5: OPAMP1: Comparison between Non-Inverting Amplifiers based on CNT-FETs with n=1, n=3, and n=5

Parameter	Unit	8-Transistor CNT-FET (1 Tube)	8-Transistor CNT-FET (3 Tubes)	8-Transistor CNT-FET (5 Tubes)
DC Gain		1.997	1.999	1.999
Input Resistance	Ω	1E12	1E12	1E12
Output Resistance	Ω	51.06	11.64	6.651
Bandwidth	MHz	2.05	3.97	4.9
Phase Margin	Degrees	-64.2	-52.5	-45.8
Power Dissipation	μW for 100 MΩ Load	55.19	64.85	67.74
Gain-Bandwidth Product (GBP)	MHz	4.094	7.936	9.795

From Table-5 in the previous page, we can see that for a non-inverting amplifier based on OPAMP1 model, as the number of SWNTs in the intrinsic channel region of the CNT-FETs are increased, all the aspects of the device shows improved results, excepting the power dissipation.

Figure 8: Phase v/s. Frequency Curve of OPAMP2 Si-MOSFET and CNT-FET with n=3

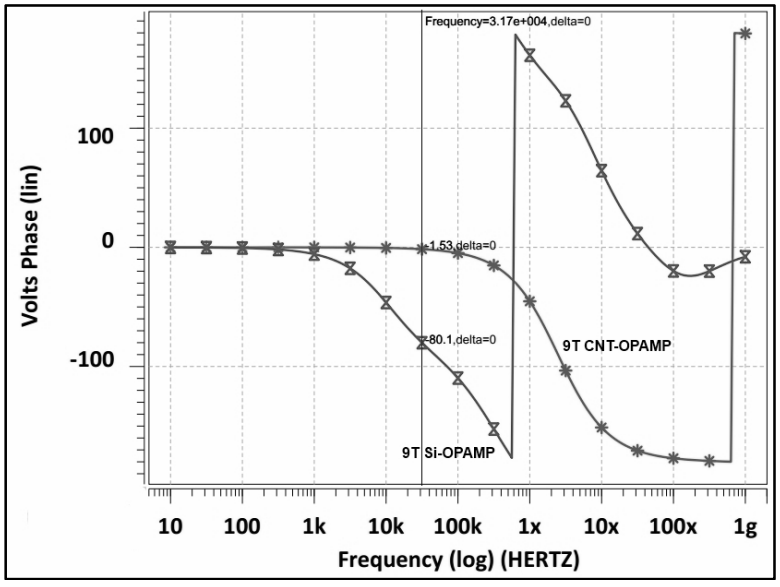


Table 6: OPAMP2: Comparison between Non-Inverting Amplifiers based on CNT-FETs with n=1, n=3, and n=5

Parameter	Unit	9-Transistor CNT-FET (1 Tube)	9-Transistor CNT-FET (3 Tubes)	9-Transistor CNT-FET (5 Tubes)
DC Gain		1.997	1.999	1.999
Input Resistance	Ω	1E12	1E12	1E12
Output Resistance	Ω	44.72	5.041	1.836
Bandwidth	Hz	661K	3.00M	5.63M
Phase Margin	Degrees	-86.1	-104	-111
Power Dissipation	μW for 100 MΩ Load	68.5	204.4	339.4
Gain-Bandwidth Product (GBP)	MHz	1.320	5.997	11.25

From Table-6 in the previous page, we can see that for a non-inverting amplifier based on OPAMP2 model, as the number of SWNTs in the intrinsic channel region of the CNT-FETs are increased, all the aspects of the device shows improved results, excepting the phase margin and power dissipation.

5. Conclusions/Implications

5.1 Limitations

The most basic limitation of our study was that under the current circumstances the physical implementation of the OPAMP was not possible and thus no practical study of either the FET or the OPAMP was achievable.

5.2 Future Prospects of the Study

In future, the extension of the study would be to physically examine the OP-AMP and understand the competence of carbon nanotube compared to the traditional CMOS technology and the influence of the environment on nanotube's performance. A physical performance observation of carbon nanotube will confirm our study to a commercial basis and will prove that Moore's law can still be valid.

5.3 Final words

Finally we can conclude from the results obtained from the simulations that carbon nanotube is far superior to silicon as a semiconducting material. In future, nanotubes will eventually replace

silicon and even the simplest, the smallest of technologies will have nanotube as its basic block. The limitation of fabrication is the only obstacle that is obstructing the growth of the carbon nanotube industry. Eventually commercialization of carbon nanotube will come to pass.

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