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A Novel Design of Reversible Programmable Read only Memory

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We have proposed a novel RPROM design. We have also proposed a reversible decoder ITS and another reversible gate TI. Our proposed design is 30.90% better w.r.t. quantum cost and 31.58% better w.r.t. number of garbage. The proposed reversible decoder is 60% better w.r.t. quantum cost than the existing ones.

Field of Research: Reversible Logic, Programmable Read Only Memory, PLA, Decoder, Quantum Cost, Garbage Output and Constant Input.

1. Introduction

Reversible logic is used in reversible circuits. The reversible circuits have various applications e.g., quantum computing, optical computing, cryptography, nanotechnology, DNA technology and low power CMOS technology. To reduce power consumption extremely, reversible logic can be used. It may be a core part for solution in future. Besides, the main dictation for reversible computing is the only way that is logically consistent with the most established principles of fundamental physics. The reversible computing provides that performance on most applications within realistic power constraints might still continue increasing indefinitely.

In the present technology, power extravagance is one of the key issues. The importance of reversible logic is increasing day by day for its significant. To get low power devices, reversible logic has become demandable way which is one of the basic reasons. When information becomes lost, then energy is also lost. It happens when an input cannot recover its output and it has been proved by Landauer (1961). He also showed that, if a bit of information is lost, then *kTln2* joules of heat generates; where *k* is Boltzman's constant of $1.38 \times 10^{-23} J/K$ and *T* is absolute temperature. To reduce energy waste, reversible circuit can be used and Bennet (1973) showed it. Reversible logic follows one-to-one mapping system followed by input number and output number remains equal. Here is no information loss and no energy dissipation. Miller et al (2003) proved that, if the number of gate increased, then it is not good metric of optimization. But, the use of reversible gate can decrease the number of gates, because one output of one gate can be used if reversible logic supports.

ROM is used to store the value which is unchangeable easily. Many research works have been done on reversible memory, but there is a few works have been done in this area. In recent years, the use of reversible gates is increasing for its major

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metric of cost optimization. There is no scope to loss the value if power is off. For this reason, it is nonvolatile. It also pro provides security because it is not possible to modify.

In this paper, we have proposed a novel design of reversible programmable read only memory (RPROM). The existing PROM is irreversible. Our proposed RPROM is efficient because in this RPROM, we have proposed a reversible decoder which has low quantum cost and no garbage output. We have also proposed a new AND plane and EX-OR plane for decreasing RPROM in which the number of garbage output and quantum cost is reduced. In this paper, we have also proposed a reversible gate called TI.

Included attributes of this paper is arranged as following: Section *2* includes the basic definitions on reversible gate and logic followed by Section *3* includes the proposed method of our work. In section *4,* experimental results are included. Finally, section *5* has conclusion of this paper.

2. Literature Overview

In this section, we have discussed about some basic definitions that will help to understand about reversible gate and logic, garbage, quantum cost, constant input and read only memory.

2.1. Reversible Gate

The equal number of inputs and outputs of a gate is referred to reversible gate. Babu et al (2004) defined that reversible gate has one-to-one mapping between input vectors and output vectors from. Reversible gate has no bit loss. If the inputs are I_t $\{I_1, I_2, I_3, \ldots, I_n\}$, then the outputs will be O_t $\{O_1, O_2, O_3, \ldots, O_n\}$.

Figure 1: Feynman Gate

Example 2.1.1: From the Figure 1, we can see that, Feynman gate has two inputs and two outputs. Mamun and Hossain (2012) have shown that Feynman gate is a *2×2* reversible gate as well as Fredkin gate is a *3×3* and Toffoli gate is a *3×3* reversible gate.

2.2. Garbage output

Garbage is the output that has no use as input for other gates. Another way we can say that,the output is needed to fulfill reversibility for a reversible gate or circuit is called garbage output.

Example 2.2.1: The garbage output of Feynman gate is expressed with * in Figure 1. Feynman (1986) showed that Fredkin gate has one and Toffoli gate has two garbage outputs.

2.3. Quantum Cost

The quantum cost of any reversible cuircuit is identified as the number of *1×1* and *2×2* or quantum gates needed to accomplish the design illustrated by Rahman et al (2011).The quantum cost of reversible Feynman gate is one, Toffoli gate is five and Double Feynman gate is two demonstrated by Rahman et al (2011). Actually the quantum cost depends on using of controlled-v, controlled-v+, NOT gate and CNOT gate showed by Rahman et al (2011) . Low quantum cost is better for reversible gate. So at present, researchers are trying to reduce quantum cost.

Example 2.3.1: Mamun and Hossain (2012) have shown that the quantum cost of Feynman gate is two.

2.4. Constant Input

Constant inputs are the inputs of reversible gate or circuit that are either set to 0 or 1.

Example 2.4.1: We will get A′ from the Feynman gate, if we give constant value 1 to B in Figure 1.

2.5. Read Only Memory

Read-only memory or (ROM) is a medium of data storage where data can only read. Data is store in ROM permanently. If the power of computer is turned OFF, the data will not be loss. ROM stored the data that helps to start a computer.

Besides, there are some properties of read only memory as following:

1. Non-volatile: The data that is stored in ROM is not removed if the power is ON or OFF. So, it is called non-volatile storage.
2. Security: The data is not removed or changed easily; as a result it provides security.

There are several kinds of ROM as following:

1. ROM- Read Only Memory.
2. PROM- Programmable Read Only Memory.
3. EPROM- Erasable Programmable Read Only Memory.
4. EEPROM- Electrically Erasable Programmable Memory.
5. Flash EEPROM memory.

2.6. Programmable Read Only Memory (PROM)

ROM was much time-consuming and expensive when ROM chips were first created. Mainly, for this reason, Yang et al (2013) made a ROM that is programmable and this ROM is known as programmable read only memory or PROM.

3. Proposed Method

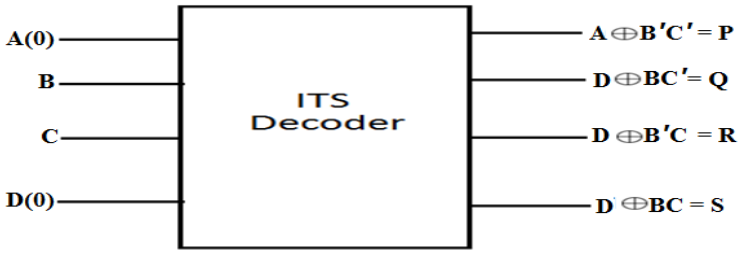
Methodology is the systematic, theoretical analysis of the methods applied to a field of study. In this section, we have discussed about decoder, our proposed design of *2 to 4* reversible decoder, proposed design of PROM that will help to understand about our novel design of RPROM.

3.1. Decoder

A decoder is a device that reverses the operation of encoder and it has multiple inputs and multiple outputs. The inputs and outputs follow the rule of *n* to 2^n . Here *n* is the number of inputs and 2^n is the number of outputs. If input becomes *n=1, 2, 3…* then output will be 2^1*=2*, 2^2*=4*, 2^3*=8...*

The binary encoded input number of a decoder is passed to ROM which is referred to as address. The address line is presented by every signal line. In this paper, we have proposed a reversible decoder named ITS decoder, which is shown in Figure 2.

Figure 2: Reversible ITS Decoder



Our proposed decoder has quantum cost of *4*, which is the lowest in the literature. The quantum representation of our proposed ITS decoder is shown in Figure 3.

Figure 3: Quantum Representation of ITS Decoder

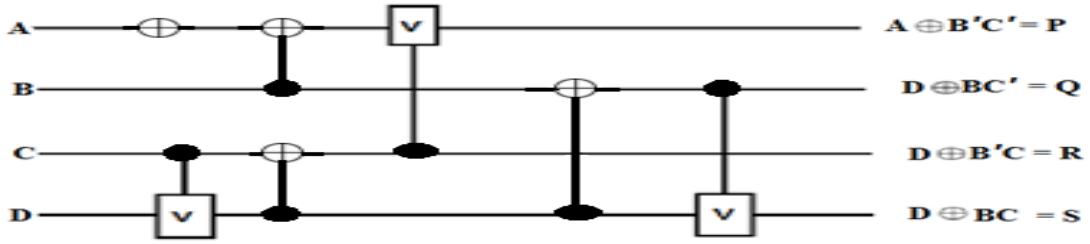


Table 1 shows the truth table of reversible ITS decoder. We get the one-to-one mapping between input vectors and output vectors from the Table 1 which showed by Babu et al (2014).

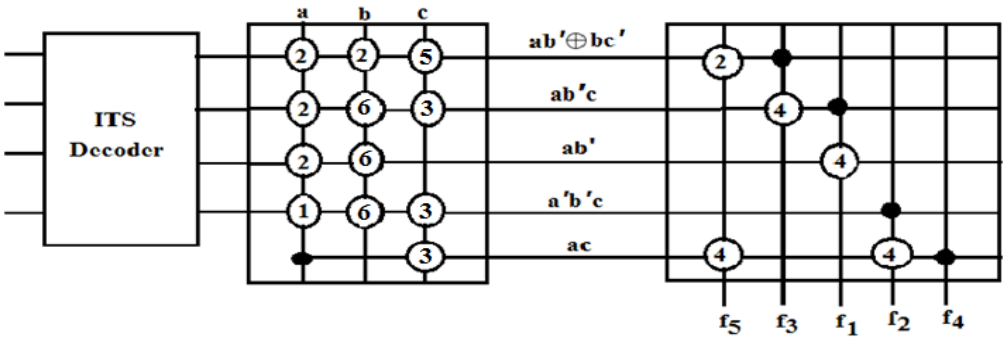
Table 1: Truth Table of Reversible ITS Decoder

A	B	C	D	P	Q	R	S
0	0	0	0	1	0	0	0
0	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0
0	0	1	1	0	1	0	1
0	1	0	0	0	1	0	0
0	1	0	1	0	0	1	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	0	0	0	0	0
1	0	0	1	0	1	1	1
1	0	1	0	1	0	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	1	0	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	1	1	0

3.2. Proposed Design of RPROM

In our proposed design of PROM, we have used our proposed decoder, AND plane and EX-OR plane. PROM uses decoder as input; as well as AND plane and EX-OR plane are used as output which is shown in Figure 4. The output of decoder is selected as AND array plane's input terms. The output of AND plane is used as EX-OR plane's input. Final output of EX-OR plane shows the output of PROM. Every line of input and output is known as address line and every bit is known as word.

Figure 4: Block Diagram of RPROM



Programmable Read Only Memory or PROM is consist of a AND plane and EX-OR plane. Where AND plane is fixed and EX-OR plane is programmable. A large number of equations can have for a PROM.

To propose our new reversible PROM we have used Feynman gate and MUX gate used by Mitra et al (2012). We have also proposed a new reversible gate named TI gate. Its quantum cost is four. Proposed AND plane and EX-OR plane is better than existing PLA of Mitra et al (2012) w.r.t. quantum cost and number of garbage

outputs. Example of the multi-ESOP (Exclusive Sum Of Product) functions are $F = \{f_1, f_2, f_3, f_4, f_5\}$. In our proposed RPROM, let us have the following functions:

f_1 = ab'⊕ab'c
f_2 = ac ⊕a'b'c
f_3 = ab'⊕bc'⊕ab'c
f_4 = ac
f_5 = ab'⊕ ac ⊕bc'

The input variables depend on products. In EX-OR plane, the products of function will be generated. We have established two algorithms for our RPROM: one is for EX-OR plane and another is for AND plane.

The proposed *3×3* reversible TI gate has been used to get new RPROM. It has been used to reduce the number of garbage outputs and quantum cost of AND plane and EX-OR plane. The quantum cost of TI gate is four and garbage is two. The TI gate is shown in Figure 5.

Figure 5: Proposed TI Gate

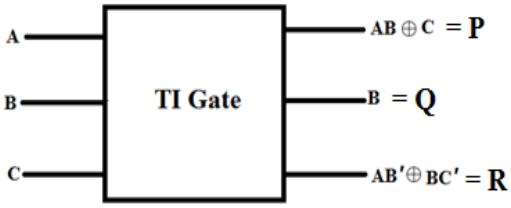


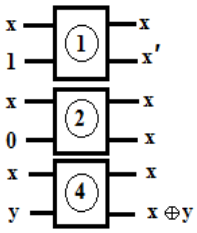
Table 2 shows the truth table of reversible TI gate. We get the one to one mapping between input vectors and output vectors from the Table 2 which showed by Babu et al (2004).

Table 2: Truth Table of Reversible TI Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	1	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	0	1	0

There exist three modes of Feynman gate which has been used for our proposed PROM: FG-1, FG-2, and FG-4 which is shown in Figure 6.

Figure 6: Different Uses of Feynman Gate for Different Purposes



One mode of MUX gate MG-3 is also shown in Figure 7. In addition, two modes of TI-5 and TI-6 gates are shown in Figure 8. POINT is used where gate is not used.

Figure 7: One Acting Template of MUX Gate

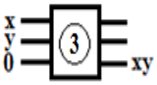
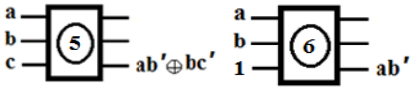


Figure 8: Two Acting Templates of TI Gate



Size of the function [*Size Of (f_i)*]: Size of the function is the number of total products that is expressed as the ESOP.

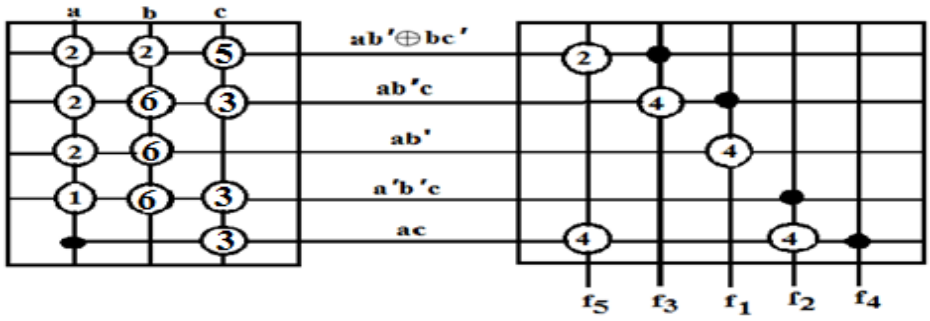
Example 3.2.1: The number of products of f_1 is 2, f_2 is *2* and $f_3$is *3*. The product of functions is shown in the Table 3.

Table 3: The Product of Functions

Functions	f_1	f_2	f_3	f_4	f_5
Number of Products	2	2	3	1	3

If anyone wants he can use more number of products and functions. In this paper, we have proposed a novel Reversible Programmable Read Only Memory (RPROM). RPROM consist of an AND plane and EX-OR plane. Reversible PLA also consist of AND plane and EX-OR plane. Researchers have done many works on reversible PLA. Existing design of the multi-output ESOP function, where $F = \{f_1, f_2, f_3, f_4, f_5\}$ showed by Rahman et al (2011).In our proposed design, AND plane and EX-OR plane is used for particular functions. We cannot compare with any reversible ROM, so that we compare with existing reversible PLA. Our proposed AND plane and EXOR plane is shown in Figure 9.

Figure 9: The Combined Design of Proposed AND Plane and EX-OR Plane



In the Proposed design, the order of output functions is related to the number of product. For EX-OR plane our proposed algorithm is following:

Proposed Algorithm for EX-OR Plane

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1. **START** TPOINT:=0 [TPOINT= total number of DOT]
2. Arrange the output function according their products.
3. **REDO** step 4 for every output function of F.
4. **IF** a single product or all products of
5. a function exits, **THEN** use FG-2.
6. **ELSE** assign product and use POINT
7. Here TPOINT:= TPOINT+1
8. **END IF**
9. For EX-OR operation, use FG-4.
10. **END IF**
11. **END**

Theorem 1: Let, the number of EX-OR operation x and y represents the number of output functions. TPOINT is the number of cross point, then the minimum number Feynman gates of EX-OR plane *is x + y - TPOINT.*

Proof: If the number of EX-OR operation x, y is the number of output function followed by TPOINT is the cross point of EX-OR plane, then the total number of Feynman gate required for EX-OR plane *is x + y – TPOINT*. In EX-OR plane the number of EX-OR operation x is 3, the number of output function y is 5 and the number of TPOINT is 4. So total number of Feynman gates of EX-OR plane is = *x + y – TPOINT = 4 + 5 – 4 = 5.*

Theorem 2: If the number of product is p and the total number cross point is TPOINT, then the garbage of EX-OR plane is *p – TPOINT.*

Proof: TPOINT is the cross point and product is p for y output function. So, the number of garbage of EX-OR plane is p – TPOINT. In our proposed EX-OR plane product p is *5* and the cross point TPOINT is *4*. So the number of garbage of EX-OR plane is *p - TPOINT = 5 – 4 = 1.*

Proposed Algorithm for AND Plane

1. **START** TPOINT:=0 [here TPOINT is the total number of POINT]
2. **REDO** step 3 to get every product .
3. **IF** is the first input of **THEN**
4. **IF** is complementary form, **THEN**
5. use FG-1
6. **END IF**
7. **ELSE**
8. **IF** input is **THEN** use FG-2
9. **END IF**
10. **ELSE** use POINT and TPOINT: = TPOINT+1
11. **END IF**
12. **ELSE IF** is complementary form **THEN** use TI-6
13. **ELSE** use MG-3
14. **END IF**
15. **IF** full product **THEN** use TI-5
16. **END IF**
17. **END**

4. Experimental Results

The comparison between the proposed and Morrison et al (2011) is shown in Table 4. The achievement of our proposed decoder is at quantum cost. The quantum cost is lower as compared to the existing decoder.

Table 4: Comparison W.R.T. Quantum Cost Between Proposed and Existing Decoder

Reversible Decoder	Quantum Cost
Morrison et al (2011)	10
Proposed	4

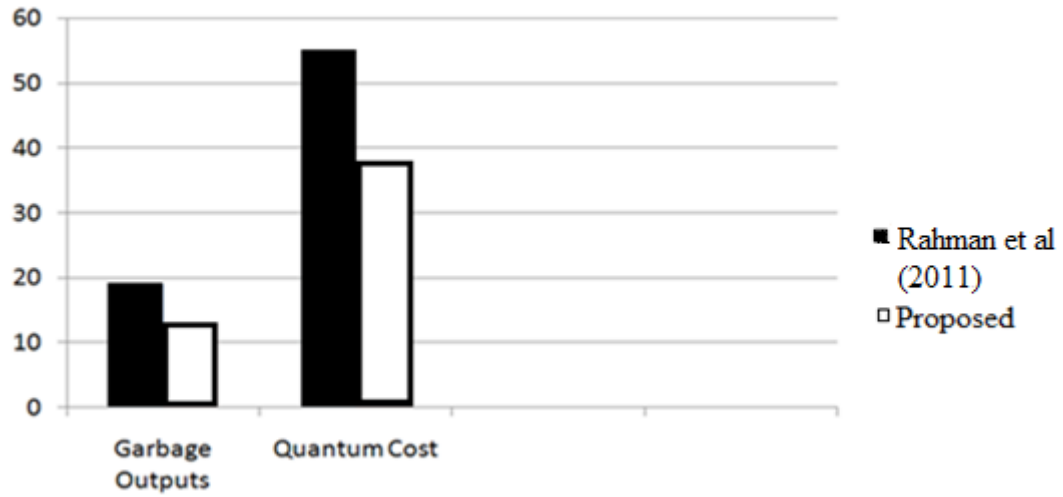
Table 5 shows the comparison between the proposed design and existing design. From the Table 5, we can see that, the proposed design is not fault tolerant where the existing design is fault tolerant.

Table 5: Comparison between Proposed and Existing Design

Design	Garbage Output	Quantum Cost
Rahman et al (2011)	19	55
Proposed	13	38

The number of total gates, quantum cost and garbage is the lower in our proposed design as compared to the existing design of Rahman et al (2011) which is shown in Figure 10.

Figure 10: Comparison between Proposed and Existing Design



5. Conclusion

Our main focus is to propose a RPROM and this is a unique research in the literature. Our proposed AND plane and EX-OR plane have lower number of garbage outputs that is 13 and lower number of quantum cost which is 38, where the best known existing method requires garbage outputs of 19 and quantum cost of 55. We have also reduced the quantum cost of reversible decoder which is 4, where quantum cost of a best known existing decoder is 10.The proposed *4×4* reversible decoder, AND plane and EX-OR plane are used to design an efficient RPROM. It is proved that, the power and the information loss is reduced by our proposed design. Our proposed design is not fault tolerant and online testable. In future, our focus is to propose a reversible fault tolerant decoder for this design as well as to propose a reversible fault tolerant programmable read only memory, since fault tolerant circuits preserve parity bits. We also want to make our design as online testable. Our proposed RPROM could be used for storing video game software and fixed data for electronic equipment, such as fonts for laser printers, dictionary data in word processors, and sound data in electronic musical instruments.

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